AN OPTIMIZED ARCHITECTURE FOR DYNAMIC RECONFIGURABLE FIR FILTER IN SPEECH PROCESSING

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ABSTRACT

In this paper, we have proposed a Dynamic Reconfiguration Scheme (DRS) for the FIR filter in which the existing multiplier of the FIR filter is replaced by the proposed Estimation Distribution Multiplier Blocks (EDMB). The important aspect of the proposed DRS is that it provides an efficient area and power optimization while implementing in hardware. To ensure the versatility of the proposed method and to further evaluate the performance and correctness of the structure in terms of area and power consumption, we have implemented the hardware in Xilinx Virtex 7 Field Programmable Gate Array (FPGA) device and synthesized with Cadence RTL Compiler using TSMC 180 nm standard cell library. The experimental analysis of the proposed reconfigurable design approach takes speech signal as the benchmark input. The analysis shows that the proposed technique is better when compared to the existing reconfiguration techniques with 43.60% power savings and 6.34% area reduction.

Keywords: Reconfigurable design, Digital signal processing, Speech signal processing, Finite impulse response filter, Area optimization, Low power design.

1.0 INTRODUCTION

Different air-interfaces are implemented on a single generic hardware platform to support multi-standard wireless communications [1]. The adjacent channel attenuation specifications of wireless communication standards are so stringent that higher order filters are required to achieve high spectral containment and/or noise attenuation. The explosive growth in mobile computing and portable multimedia application, has increased the demand for low power Digital Signal Processing (DSP) systems. One of the most widely used important building blocks of DSP system is Finite Impulse Response (FIR) filter. Reconfigurability, low complexity and low power are the key requirements for FIR filters employed in multi-standard wireless communication systems. FIR Digital filter are used extensively in mobile communication systems such as channelization, channel equalization, interference cancellation, spectral shaping, matched filtering and pulse shaping due to their absolute stability and linear phase properties. Recently, with the advent of Software Defined Radio (SDR) technology, FIR filter research in DSP has been focusing on reconfigurable realizations. Since the ultimate aim of the future multi-standard wireless communication receiver is to realize its functionalities in mobile handsets, where its full utilization is possible, the low power and low area implementation of the FIR channel filters are inevitable.

Speech is an immensely information-rich signal formed by either frequency, amplitude or time modulated carriers to convey information about words, speaker identity, accent, expression, style of speech, emotion and the state of health of the speaker. Digital Filters are used to filter the audio data stream and increase the reliability of speech signal. Specific frequency ranges may be removed or boosted using digital filters in an audio file in order to make the audio file more realistic and pleasant to the human ear. The FIR filter finds tremendous usage in signal processing areas which includes speech processing, spectrum analysis, media communications and low-pass filtering.

To evaluate the performance of the proposed technique, we have coded the proposed technique and the existing algorithms [2,3,4,5,6] in MATLAB and Verilog HDL. We have synthesized and implemented the proposed and the existing techniques in Xilinx Virtex 7 XC7V585T-2LFFG1761C device (Xilinx, Inc., San Jose, CA, USA) [7] and Cadence RTL Compiler [8] using TSMC 180 nm standard cell library.

The paper is organized as follows: Section 2 presents a survey of existing low power and low area reconfigurable techniques for finite filtering. In section 3, the motivation of the proposed work is discussed. The proposed Dynamic Reconfiguration Scheme (DRS) architecture is presented in section 4. The discussion of the experimental analysis of the proposed method is done in section 5. Finally, section 6 concludes the paper with future work ideas.

2.0 RELATED WORK:

In this section, various area reduction and power saving techniques for reconfigurable architectures of FIR filters, are discussed. Fig.1 shows the various types of FIR filter design and their characteristics. Efficient structures for the implementation of loop filters within FPGAs is discussed by Yair Linn et al. [9]. The limitation of the loop filter method is that, the complexity of FIR filters is dominated by the complexity of coefficient multipliers. Hartley et al., [10] have presented the Common Subexpression Elimination (CSE) methods based on Canonical Signed Digit (CSD) coefficients that produce low complexity FIR filter coefficient multipliers. The limitation of Hartley et al.,[10] technique is that the determination of the gain by subexpression sharing in hardware is complicated. R. Pasko et al., [11] have proposed a method for solving Multiple Constant Multiplication (MCM) by modified 2-bit CSE technique. The limitation of MCM is that the input is multiplied with a constant value and it requires large number of logic gates, which in turn, results in hardware complexity. A Non Recursive Signed Common Subexpression Elimination (NR-SCSE) technique proposed by Marcos Martínez-Peiró et al.,[12,13] increases the speed of operation by minimizing the Logic Depth (LD). But this is done at the cost of accuracy and hence it is not widely used. This limitation is overcome in the technique proposed by R. Mahesh et al., [14] in which the authors have made use of the Binary Common Subexpression Elimination (BCSE) method which provides improved adder reductions but the there is a need for large power requirements.

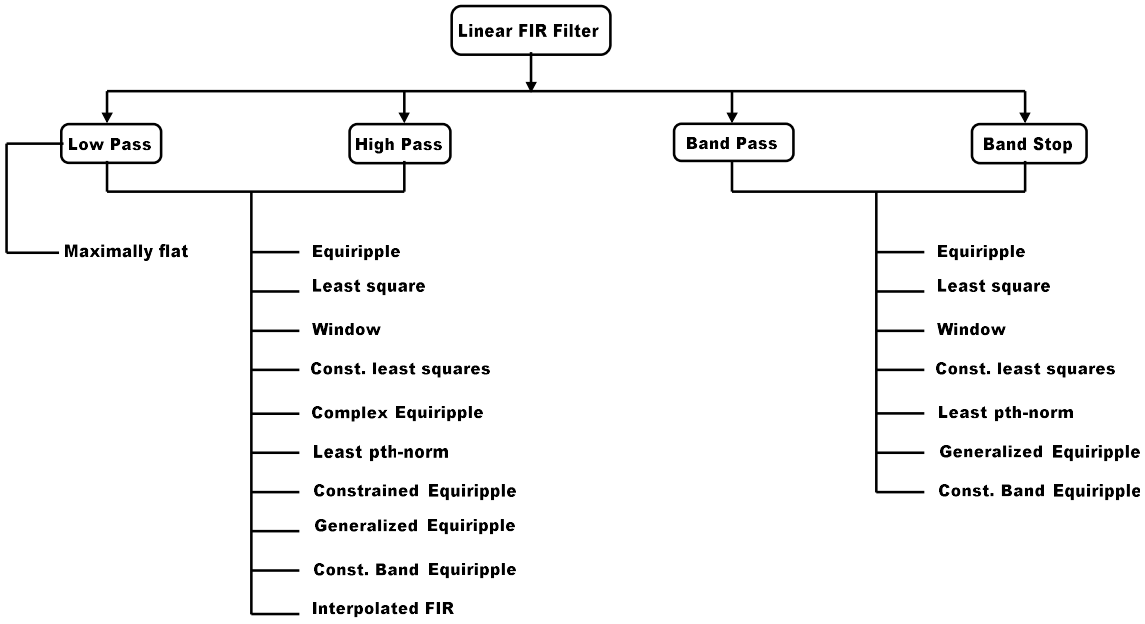


Fig. 1: Various linear FIR filter and its characteristics

Several low power implementation approaches for reconfigurable FIR filters have been proposed in literature [15-21]. A method based on the pseudo floating point is introduced by A. P. Vinod et al., [15] which encodes the filter

coefficients and reduces the complexity of the filter, but here there is a limitation in filter lengths. The main disadvantage of the filter processors is that the area and power requirements are significantly large. A CSD based digit reconfigurable FIR filter architecture proposed by Kuan-Hung Chen et al., [3] demands huge hardware resources. The high speed programmable CSD based FIR filter architectures discussed in [16-20] are appropriate only for relatively lower order filters and are not suitable for filters of higher order. Although, few works in the literature addressed the problem of reducing the complexity of coefficient multipliers in reconfigurable FIR filters, these were limited to low order filters and hardly any work has demonstrated the reconfigurability in higher order filters. There is a need for developing an efficient complexity reduction technique for higher order reconfigurable filters especially for speech signal applications.

The coefficient multiplication methods like Multiple Constant Multiplication (MCM) [27], Constant Shift Method (CSM) and Programmable Shift Method (PSM) [28] consider the coefficients as constants and input signal as variable. The advantage of CSM is that it produces high-speed filters at the cost of a slight increase in area and power consumption. On the contrary, the PSM produces filters with low area and power consumption at the cost of increase in delay.

H. Samueli et al., [29] and O. Gustafsson et al.,[30] describe the power consumption reduction in FIR filter, which focus on the optimization of the filter coefficients while maintaining a fixed filter order. Low power digital filters described by Jeffrey T. Ludwig et al., [2] and Amit Sinha et al., [32] are constructed from approximate signal processing technique [31]. The digit reconfigurable FIR filter proposed by Kuan-Hung Chen et al., [3] and reduced representation of 2's complement representation proposed by Zhan Yu et al., [4] are realized in various frequency responses using a single filter by coefficient decimation approach. In all the above works [29-36], large overhead is incurred to support reconfiguration, because in FIR filtering the input and output signals are multiplied by predefined constants, to exploit the redundant multiplications.

Reconfigurable FIR filters for dynamic power consumption have been introduced by Seok-Jae Lee et al., in [34]. This method is not suitable for real time input varying speech samples, because here the threshold is fixed for both input samples as well as the filter coefficients and this results in the degradation of filter performance. Jiajia Chen et al.,[37] proposed an efficient Reconfigurable Constant Multiplier (RCM) technique, which achieves greater hardware savings but is limited by the latency of the subsystem. This limitation has been overcome by a new design for the programmable FIR filters proposed by Jiajia Chen et al., in [38], which uses Extended Double Base Number System (EDBNS). Albeit the reduction of logic complexity and the critical path [34], [37] and [38], the hardware reduction for 8-bit coefficient filters are not significant. The above limitations have been addressed and a suitable solution has been designed in the proposed dynamic reconfiguration scheme, which would provide more suitability for the employment of the proposed method for improving the filter performance.

3.0 MOTIVATION FOR THE PROPOSED SCHEME

The emergence of demanding applications like image, audio/video processing and coding, sensor filtering, etc. where in the power, speed, performance, system compatibility and reusability plays a major role which makes the design of reconfigurable architectures imperative. The following are the problems of the existing reconfigurable FIR filter techniques:

1. The threshold value is fixed for both the speech and sound samples input as well as the filter coefficients input. This method gives power saving but there is a degradation in filter performance in terms of Mean Square Error (MSE).
2. In the existing methods, multiplier-shifter by data processing unit [3], low power partial product generation by compensation vector approach [4] and truncated multiplier [34] are used. In [3], zero, plus and shift signals are given as input to the data processing unit which performs the multiplication. The control signals are generated in serial in parallel out fashion. The multiplication result depends wholly on the three signals mentioned above. The above method is not suitable for higher order filter. Compensation vector approach discussed in [4] uses several logic gates which in turn leads to hardware complexity. In [34], the 4 bits of the LSB are truncated, when the input samples as well as the filter coefficients are of high value. Thus this results in loss of information and hence inaccurate output which in turn leads to poor performance. For example, if the input is of 16 bit each, the output from the truncated multiplier is 24 bits instead of 32 bits, and hence leads to improper filtering.
3. Constant threshold is fixed for all characteristics of filter such as Low pass equiripple, least square and

window. This makes it difficult to distinguish the individual characteristics of each category of filter.

4. There is a significant overhead in the existing techniques, which makes use of the flip-flops, amplitude detectors, control signal generator and the modified gates for turning off the multipliers.
5. A window named Multiplier Control Signal Decision window (MCSD) is fixed for monitoring the filter coefficients and the taps are decided by control signal generator. MCSD window restricts the switching but the size of the window [equal to 4] is fixed throughout the analysis. Taps are monitored only for those coefficients present inside the MCSD window. Window size is not varied. When the taps are increased, monitoring of all filter coefficients is essential for improving the filter performance.
   All the above drawbacks have been addressed in the proposed Dynamic Reconfiguration Scheme (DRS) using the Estimation Distribution Multiplier Block (EDMB) and a suitable solution has been suggested for the same.

4.0 PROPOSED DRS USING EDMB:

In the design of digital FIR filter, the multiplier block occupies a larger area when compared to the adder structure. For obtaining an area optimized design for FIR filter, we have proposed an Estimation distribution multiplication technique. The proposed FIR filter is realized as Low pass type in transposed form structure. Different characteristics of the filters namely Equiripple, least square, window based techniques are considered. Further the Hamming and Bohman windows are also considered with varying stopband (W_s) and passband frequencies (W_p) normalized from 0 to 1. We have designed a 25, 50 and 75 taps reconfigurable FIR filters in the proposed method. The proposed reconfigurable FIR filter is shown in Fig.2.

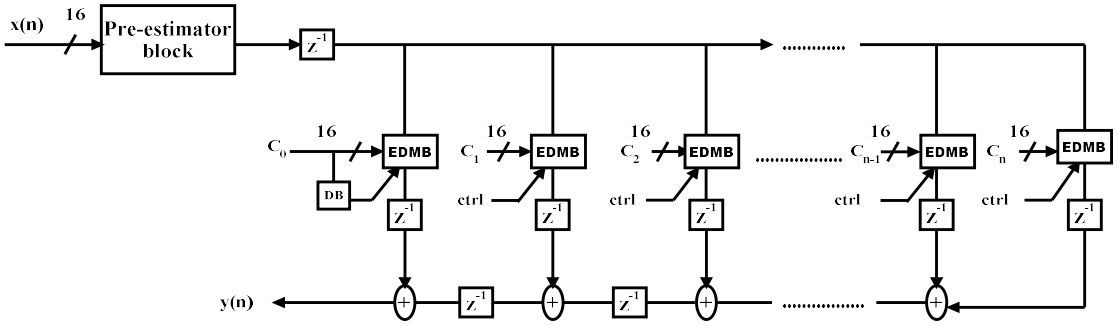


Fig. 2: Proposed reconfigurable FIR filter with Estimation Distribution Multiplication Block (EDMB)

The data inputs X(n) of the filter, that have large variation in amplitudes, are multiplied with the coefficients which also have large variations in amplitude. The basic concept of the proposed technique is that when the amplitudes of inputs given to a multiplier namely, the data input and filter coefficient input are small, the resulting product will also be proportionately small and this in turn, implies that the corresponding multipliers can be turned off. Furthermore, this process will have a negligible effect on the filter performance.

Now let us consider the scenario where the input to the multiplier of the FIR filter are two negative values. In this case, multiplication of two negative values gives rise to large switching activities, due to the series of 1's in the MSB part representing the negative value. By cancelling the multiplication of two small numbers, considerable power savings can be achieved with negligible filter performance degradation. In order to incorporate the above concept in the proposed scheme, we have designed the multiplier in such a way that when the filter coefficient C is less than the filter coefficient threshold C_{th}, the multiplier shall be turned off. On the other hand, when the filter coefficient C is greater than or equal to the filter coefficient threshold C_{th}, the multiplier is turned on. Thus the proposed reconfigurable DRS based FIR filter dynamically changes the filter order.

In the proposed reconfigurable DRS technique the multiplier block in the filter design is replaced by Estimation Distribution Multiplication Block (EDMB). The EDMB consists of Pre-Estimator block (PEB), Selection Block (SB), and finally adder block. These sub blocks are explained in the following subsections.

4.1 Area Efficient Multiplier-less Estimation distribution unit:

The vector scaling operation performs the multiplication of vector and scalar. The coefficients are represented in the form of vectors. The vector units are called as alphabets. The group of alphabets are called as alphabet sets. The alphabet sets are the common units. Whenever these units occur, the values which are pre-estimated will be distributed to the units needed. The filters considered for the design includes 25 taps, 50 taps and 75 taps (low pass) equiripple, least square and window characteristics. Further the Hamming window and Bohman window characteristics with different pass band and stop band frequencies are also considered for analysis.

4.1.1 Decision Block:

In order to monitor the amplitudes of filter coefficient samples and cancel the multiplication operations, Decision Block (DB) is used and its block diagram is shown in Fig. 3. The filter coefficient (C_{th}) threshold is fixed by considering the average of all filter coefficients. The design of DB is dependent on the coefficient threshold. The filter coefficient threshold C_{th} is changed adaptively depending upon the designer's considerations. DB is implemented using a simple comparator. When the filter coefficient C is less than the filter coefficient threshold C_{th}, the control signal (Ctrl) value is made as '1' and the multiplier is turned off. When the filter coefficient C is greater than or equal to the filter coefficient C_{th} threshold, the Ctrl value is made '0' and the multiplier is turned on. Depending upon the incoming real time input, the Ctrl signal is generated by the decision block. The Ctrl signal is responsible for the on and off of multiplier.

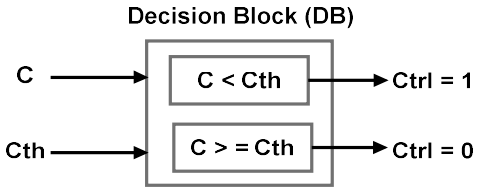


Fig. 3: Decision block (DB) block diagram (where C is the filter coefficient and C_{th} is the filter coefficient threshold)

The overall block diagram of Proposed Pre-Estimation Distribution block is shown in Fig. 4. The proposed PEB gives the estimation values of all the filter coefficients. The filter coefficient values can be pre-estimated and are placed in the PEBs.

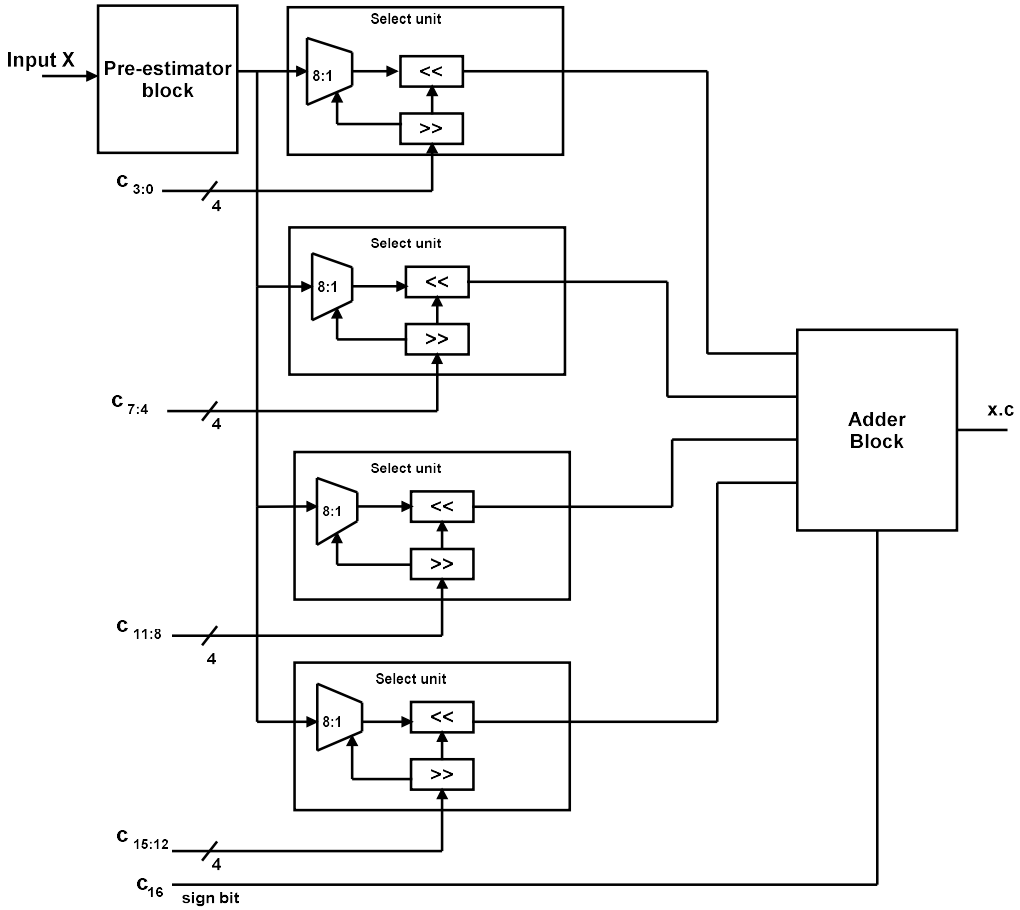


Fig. 4: Overall block diagram of Pre-Estimation Distribution block

4.1.2 Pre-estimator Block:

We have proposed a pre-estimator that performs the multiplication of only the repeated bits of alphabets with the input sample. The major significance of using a Pre-estimator is that it lowers the complexity of the design. Since alphabets are small bit sequences, the multiplication with input X and alphabets can be done without compromising the performance. Once the number of multiplications of alphabets with input X are calculated by the pre-estimator, the outputs are distributed to all the Selection Blocks (SBs), which reduces the computational complexity of the filter. This is the main significance of the proposed EDMB as it removes the redundant multiplications, which in turn, has an effect on the filter performance in terms of area reduction and power saving. The FIR filter coefficients are fixed for individual characteristics of the filter. For example, the 25 taps equiripple FIR filter will have the filter coefficients as C(0) = 11111101, C(1) = 00000011, likewise all the other coefficients are taken. Half of the filter coefficients values will be repeated because of linear symmetric characteristics of the FIR filter. In case of 25 taps FIR filter, the coefficients C(0) to C(11) will be repeated for the coefficients from C(13) to C(24). The value of the filter coefficient C(24) will be same as the filter coefficient C(0) and the value of the filter coefficient C(23) will be same as the filter coefficient C(1) and so on. The centre filter coefficient C(12) will have the maximum value. Hence, the pre-estimate values can be calculated only for the coefficients ranging from C(0) to C(12). After

analysing various filter coefficients with respect to the FIR filter characteristics and in order to cover every possible coefficients and perform general multiplication operation between the sample input and the filter coefficient input, eight alphabets {1, 3, 5, 7, 9, 11, 13, 15} are chosen.

4.1.2.1 Calculation of Pre-Estimates:

The Pre-Estimates can be obtained by dividing the coefficient of 8 bits as two 4 bit values. The individual 4 bit values are termed as alphabets. The group of alphabets form an alphabet set.

Consider the 25 tap low pass equiripple characteristics with pass band frequency (W_p = 0.10) and stop band frequency (W_s = 0.38) normalized from 0 to 1. The first ten filter coefficients of the 25 tap low pass equiripple filter is expressed in binary values as follows:

C(0) = 00000000; C(1) = 00000001; C(2) = 00000010; C(3) = 00000011;C(4) = 00000110
C(5) = 00001000; C(6) = 01011111; C(7) = 01110110; C(8) = 11110001; C(9) = 11111101

The alphabets are C(1) [3:0] = 0001, C(2) [3:0] = 0010, C(3) [3:0] = 0011, C(4) [3:0] = 0110,
C(5) [3:0] = 1000, C(6) [3:0] = 1111, C(6) [7:4] = 0101, C(7) [7:4] = 0111, C(9) [3:0] = 1101.

The alphabets are taken as 4 bits from each filter coefficient but the redundant bits are avoided.

The alphabet set for the above FIR filter specification is given below:
Alphabet set: {0001, 0010, 0011, 0110, 1000, 1111, 0101, 0111, and 1101}

The multiplication of the input with first four filter coefficients of low pass equiripple FIR filter is described below:

$C(0).X = 00000000.X = 2^0.(0000).X$ (1)
$C(1).X = 00000001.X = 2^0.(0001).X$ (2)
$C(2).X = 00000010.X = 2^1.(0001).X$ (3)
$C(3).X = 00000011.X = 2^0.(0011).X$ (4)
$C(4).X = 00000110.X = 2^1.(0011).X$ (5)
$C(5).X = 00001000.X = 2^3.(0001).X$ (6)
$C(6).X = 01011111.X = 2^0.(1111).X + 2^4.(0101).X$ (7)
$C(7).X = 01110110.X = 2^1.(0011).X + 2^4.(0111).X$ (8)
$C(8).X = 11110001.X = 2^0.(0001).X + 2^4.(1111).X$ (9)
$C(9).X = 11111101.X = 2^0.(1101).X + 2^4.(1101).X$ (10)

In the above example the alphabet set (0001) is used for computing C(1).x and C(8).x . Likewise it is shared by C(17) and C(24), because of the linear symmetric filter coefficients.

Let X = 00000100, C(9).X = 11111101.00000100 = 1012.
C(9).X can be expressed as shown in eqn (10), $2^0.(1101).X + 2^4.(1101).X$ 2□4□. 1111□.X+ 2□0□ 1101□.X = 13(4) +16(15)(4) = 1012 by shifting the bits.

Structure of PEBS for 25 tap low pass equiripple filter characteristics with passband frequency (W_p) : 0.10, stopband frequency (W_s) : 0.38 normalized from 0 to 1 is shown in Fig.5. The Pre-estimates performs {x, 3x, 5x, 7x, 9x, 11x, 13x, 15x} multiplications as discussed in section 4.1.2. This is implemented by using carry select adder.

4.1.3 Selection Block (SB):

The proposed SB consists of Shifter, Ishifter, Multiplexer and an adder. Fig.6 shows the proposed select unit blocks. One input to the selection unit is the filter coefficient. If the coefficient is 8 bits, then it is divided into two 4bit units and each 4 bit is given to the selection block. The 4 bit coefficient is given to the shifter. The shifter performs the right shift operation. The right shifting is performed till 1 is encountered in the Least Significant Bit (LSB). The number of shifts are monitored and the number is given as input to inverse shifter (ishifter). Two outputs emerges from the shifter block. One output is the number of shifts and another is the Most Significant Bit (MSB) bits, which

act as select line for the multiplexer. The multiplexer selects one input alphabet from the given alphabet set. The output from the multiplexer is given to the ishifter, which performs the inverse operation of shifter. Left shift operation is done till 1 is encountered in the MSB. Similar operation is performed in another set of filter coefficient (4 bits).

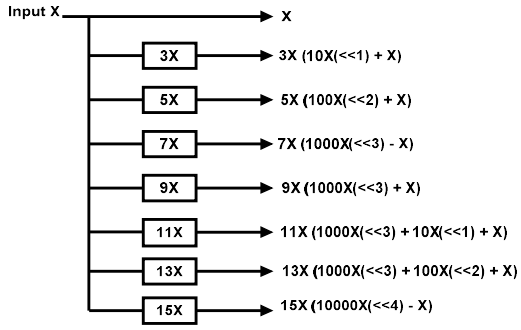


Fig. 5: Proposed Pre-Estimator block

Finally carry select adder is used to perform addition operation for the bits from the select unit. The result obtained is the multiplied value of the input sample and the filter coefficient.

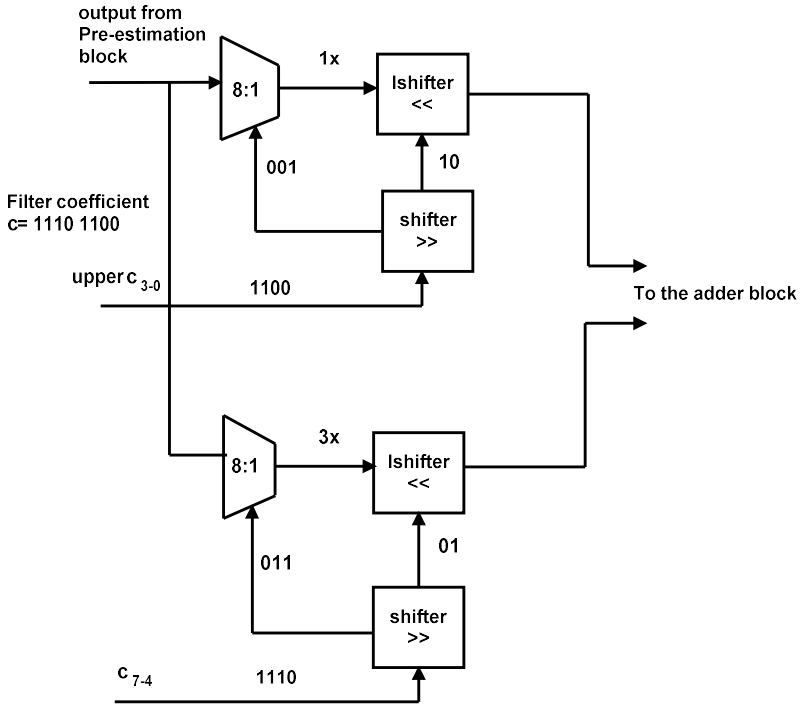


Fig. 6: Proposed Select unit block

4.1.4 Adder Block:

The carry select adder logic formulation is based on data dependence, optimized Carry Generator (CG) and Carry Select (CS) design technique used in the proposed method, helps in achieving less Area Delay Product than the existing methods. The logic optimization depends on redundant operation in formulation, but the adder delay mainly

depends on data dependence. The redundant logic operations and data dependence are identified and they all are removed.

The carry select adder structure shown in [35] consists of one Half Sum Generation (HSG) unit, one Full Sum Generation (FSG) unit, two CGs (CG_0 and CG_1) for input carry '0' and '1' respectively. The HSG receives two n-nit operands, (here n = 32) and generate half-sum word S_0 and half-carry word C_0 of width n-bits each. Both CG_0 and CG_1 receive S_0 and C_0 from the HSG unit and generate two n-bit full carry words C_1^0 and C_1^1 corresponding to input carry '0' and '1' respectively.
The logic circuits of CG_0 and CG_1 are optimized for fixed carry input bits by reducing the adder structure. The Carry Select unit selects one final carry word from the two carry words available at its input line using the control signal C_{in}. When C_{in} = 0, it selects C_1^0; otherwise C_1^1 is selected. The CS block can be implemented using an n-bit 2-to-1 MUX. Whatever may be the value of $S_0(i)$ and $C_0(i)$, for $0 <= i <= n-1$, the value of $C_1^1(i) = 1$, if $C_1^0(i) =$ '1'.

The above condition is used for the optimized implementation of CS block. The MSB of the final carry is sent to output as C_{out} and the (n-1) LSBs are XORed with (n-1) MSBs of half sum in FSG, and the final sum of (n-1) MSBs is obtained. Finaly the LSB of S_0 is XORed with C_{in} to obtain LSB of S.[35] . Hence the multiplier results are added using the carry select adder to obtain the filtered output.

5.0 ANALYSIS AND RESULTS

5.1 Proposed DRS Analysis

The proposed Dynamic Reconfiguration Scheme (DRS) overcomes the problems of the existing methods as discussed in the section 3 of this paper. The detailed analysis of the proposed scheme is presented below as cases:

Case 1: 2^{-7} is the threshold set for both, the input (X_{th}) and the filter coefficient (C_{th}) of the Reconfigurable FIR filter in the existing techniques. In this paper, FIR filter is realized as linear symmetric filter in which half of the filter coefficients are replicated. For example, in 25 taps FIR filter, the filter coefficients from C(13) to C(24) will be the same as that of the filter coefficients from C(0) to C(11). Further the average of all the filter coefficients is taken as the threshold.

Case 2: The proposed Estimation Distribution Multiplier Block (EDMB) will not truncate the LSBs and it does not depend on control signals. In the proposed EDMB the actual multiplication result is obtained. Moreover, the area occupied by the proposed multiplier is less when compared to the existing multipliers as shown in Table.1. All the designs are simulated in 180nm technology. Existing techniques with multipliers namely [3], [4], [34] are considered for analysis in this paper, since the designs are based on the low power design of the FIR Filter. As the remaining existing techniques are based on the adaptive filtering by distributed arithmetic technique and look up table technique, they are not considered for comparison with the proposed technique. The multiplication error values are also tabulated for the proposed and the considered existing techniques. For example, the multiplicand, multiplier and the multiplication values are expressed in binary as well as in decimal value. Multiplicand input (a) = 01101010 (106), multiplier input (b) = 01111100 (124), calculated multiplication result c = a * b; actual result (d) = 0011001101011000 (13144). The error value is the difference between the desired multiplication result and the calculated multiplication result. No error value is obtained for the proposed EDMB architecture, since all the alphabets are considered for calculating the multiplication result.

Table 1: Performance analysis of the proposed and existing multiplier

Multiplier type	Tech [µm]	Area [mm^2]	Total power consumption [mW]	Calculated multiplication result in binary (decimal value) (c)	Difference (d – c)	Error
Proposed method [fig. 2] EDMB	0.18	0.253	0.7502	0011001101011000 (13144)	(13144-13144)	0
Seok et al. [34] Truncated multiplier	0.18	1.018	2.1081	0010111100000000 (12032)	10001011000 (13144-12032)	1112
Chen et al. [3] Multiplier -shifter	0.18	4.956	8.1384	0011001101011000 (13144)	(13144-13144)	0
Yu et al. [4] Partial product generation by compensation vector	0.18	8.671	6.8649	0011001101011000 (13144)	(13144-13144)	0

From Table 1, it is inferred that the area utilized by the proposed EDMB is less when compared to the existing techniques because the number of logic gates used is less which makes the multiplication result computation faster. The area utilized by the proposed EDMB is 0.253 mm^2. Further the power consumption of the proposed EDMB is minimum and its value is 0.7502 milli watts.

Case 3: The threshold is made constant for all the characteristics of filter in the existing techniques. This leads to large variation in filter performance. For analysis, the real-time input speech and sound samples are taken. The speech and sound samples are processed by streaming. In case of real time input samples, the filter threshold has to be varied depending upon the characteristics of the filter. The input sample threshold cannot be same as filter coefficient threshold and it cannot be fixed for a particular input speech as well as sound sample. In the proposed technique, threshold is fixed only for the filter coefficients. The filter coefficient threshold is varied depending upon the characteristics of FIR filter, since the individual filter characteristics are unique. The threshold is fixed for individual FIR filter characteristics by finding the average of all filter coefficients which makes the filtering accuracy high.

Case 4: Multiplier Signal Control Decision window monitors the input samples and prevents the instant switching on and off of the multiplier. By fixing the value of the window say m = 3, 4, 5, all the filter coefficients are not monitored. First few samples alone are considered and accordingly the multiplier is turned on and off. For reconfiguration, all the filter coefficients has to be observed. Since linear characteristics filter is used, in the proposed method first half of the coefficients are examined. For example, in case of 25taps FIR filter, the first 12 coefficients from C(0) to C(11) are monitored along with the center coefficient C(12) which in turn improves the performance of the proposed DRS FIR filter.

5.2 Parameters for Comparison

In this section, design considerations on the proposed reconfigurable FIR filter is presented.

In following discussions, as a metric of power savings, Power Consumption ratio (P_r) is used. P_r is defined as the ratio of the reconfigurable filter's power consumption to the existing filter's power consumption.

$$P_r = (P_{proposed\ reconf} / P_{existing\ reconf}). \quad (11)$$

$$\text{Power Saving Ratio (PSR)} = (1 - P_r)\ \%. \quad (12)$$

Area reduction ratio (A_r) is defined as the ratio of the reconfigurable filter area to the existing filter area.

$$A_r = (A_{\text{proposed reconf}} / A_{\text{existing reconf}}). \quad (13)$$

Area Saving Ratio (ASR) = $(1 - A_r)$ %. (14)

Mean-Square Error (MSE) is considered as the measure of filter performance degradation which is defined as the difference between the proposed reconfigurable filter output and original filter output.

The most important factors that have a large effect on the proposed filter performance and power consumption are the threshold values of the filter coefficients. When C_{th} is set too large, it can give rise to large power savings with considerable distortion in the filter output. On the other hand, if C_{th} is too small, power savings become trivial.

5.3 Design Considerations for the Proposed DRS:

The following are the specifications of the FIR filters implemented in this paper:

- The Input sequence and coefficients are of 16- bit data.
- The FIR filter outputs are quantized and the output is 32 bit.
- The filter coefficients are obtained from the MATLAB Filter Design Analysis (FDA) tool.
- ITU test signals for telecommunication Rec. ITU-T P.50 and NOIZEUS - a noisy speech corpus database are used [39].
  * Artificial voices of American English (16 voices), real speech recordings in .wav format are taken from ITU database.
  * 30 noisy speech sentences are taken from NOIZEUS speech corpus database in .wav format
- The average of all the filter coefficients are fixed as the threshold value C_{th}.
  - 75taps lowpass equiripple with $W_p = 0.10$, $W_s = 0.20$ normalized (0 to 1) , $C_{th} = 4798$,
  - 75taps lowpass equiripple with $W_p = 0.10$, $W_s = 0.135$ normalized (0 to 1), $C_{th} = 5045$,
  - 75taps lowpass equiripple with $W_p = 0.10$, $W_s = 0.12$ normalized (0 to 1), $C_{th} = 5045$.

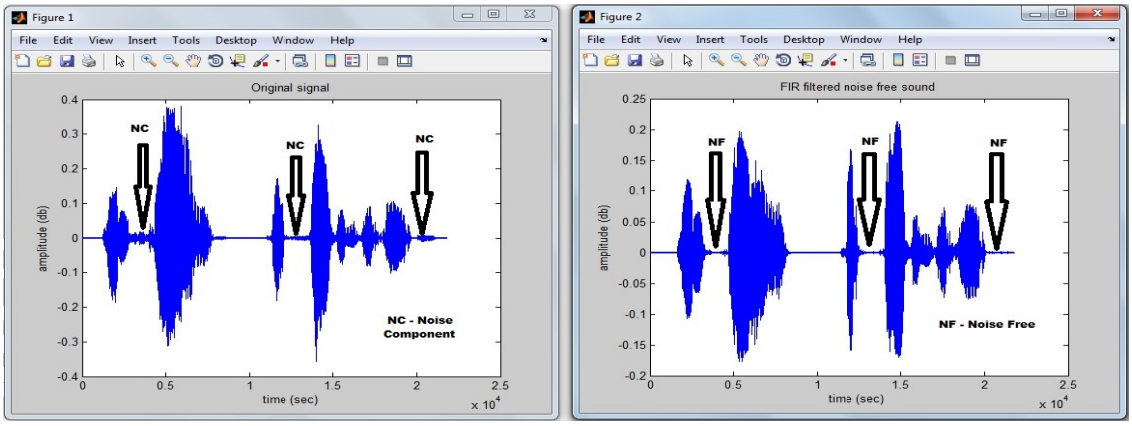
5.4 Implementation details and Result Analysis of Proposed DRS:

The proposed reconfigurable FIR filters are verilog coded and synthesized using TSMC 0.18µm CMOS technology. Power consumption is measured in Cadence Virtuoso with the operation frequency of 100 MHz, 5 V supply voltage.

5.4.1 Application to Speech Signal Filtering

Fig.7 shows the MATLAB simulation result of the proposed reconfigurable FIR filter. One of the input sample is taken from NOIZEUS speech database. The noisy database contains 30 IEEE sentences (produced by three male and three female speakers) corrupted by eight different real-world noises at different SNRs. The second input noise sample is taken from the AURORA database and includes the suburban train noise, babble, car, exhibition hall, restaurant, street, airport and train-station noise. It includes all phonemes in the American English language. The sentences were originally sampled at 25 kHz and down sampled to 8 kHz. NOIZEUS signal named sp06.wav is given as input and its filtered output is tabulated for various characteristics of low pass FIR filter. sp06.wav is 42.6 KB size with 128 kbps bit rate.

Fig.7 (a) shows the Original speech signal sp06. wav from the NOIZEUS speech database which contains Noise component (NC) in between the phonemes. Our proposed DRS filter using EDM block, effectively filters the noise component and the original signal is reconstructed. The meaning of the sentence uttered is clearly audible. Fig.7 (b) shows the Noise Free (NF) speech signal output from our proposed Dynamic reconfigurable FIR filter with EDM block for low pass equiripple 75 taps Bohman window type with the cut-off frequency of 0.12.



(a) **(b)**

Fig. 7: MATLAB result for the speech signal. (a) Original speech signal sp06. wav from the NOIZEUS speech database; (b) output from the proposed reconfigurable FIR filter with low pass equiripple characteristics Bohman window type filter with cut-off frequency 0.12.

5.4.1.1 ASIC Implementation

The Field Programmable Gate Array (FPGA) verified register transfer language (RTL) code is simulated and synthesized using Cadence encounter RTL complier using TSMC 180 nm standard cell library [8]. The supply voltage of the CMOS is fixed at $V_{DD} = 5$ V during the estimation of area and power consumption. The design is realized up to the synthesis and place and route levels leading to the estimated results is tabulated in the Table. [2-5]. For the sake of analysis we have considered the results presented in paper [34] and have compared the same with the results of the proposed scheme. It may be noted that we have considered only the results of paper [34] for analysing the power saving ratio (1-P_r) %, this is because all the other existing works are based on low power implementation and not on the dynamic reconfiguration by monitoring the filter coefficients. Hence they cannot be taken for comparison with the proposed scheme.

The graphs [Fig. 8 & 9] show the comparison of the proposed technique with various FIR filter characteristics and they are named as EQ1, LS1, EQ2, LS2, EQ3, LS3, Hamming and Bohman characteristics. The reason for chosing one particular stop band and pass band frequency for each filter characteristics is to get the accurate filtered result. The description of each characteristics is as follows:

***EQ1 – Equiripple type FIR filter** - 25 taps filter with $W_p = 0.10$, $W_s = 0.38$ normalized from 0 to 1, 50 taps filter with $W_p = 0.10$, $W_s = 0.26$ normalized from 0 to 1 and 75 taps filter with $W_p = 0.10$, $W_s = 0.20$ normalized from 0 to 1 are considered for analysis.
***LS1 – Least square type FIR filter** - 25 taps filter with $W_p = 0.10$, $W_s = 0.38$ normalized from 0 to 1, 50 taps filter with $W_p = 0.10$, $W_s = 0.26$ normalized from 0 to 1 and 75 taps filter with $W_p = 0.10$, $W_s = 0.20$ normalized from 0 to 1 are considered for analysis.
***EQ2 – Equiripple type FIR filter** - 25 taps filter with $W_p = 0.10$, $W_s = 0.20$ normalized from 0 to 1, 50 taps filter with $W_p = 0.10$, $W_s = 0.155$ normalized from 0 to 1 and 75 taps filter with $W_p = 0.10$, $W_s = 0.135$ normalized from 0 to 1 are considered for analysis.
***LS2 – Least square type FIR filter** - 25 taps filter with $W_p = 0.10$, $W_s = 0.20$ normalized from 0 to 1, 50 taps filter with $W_p = 0.10$, $W_s = 0.155$ normalized from 0 to 1 and 75 taps filter with $W_p = 0.10$, $W_s = 0.135$ normalized from 0 to 1 are considered for analysis.
***EQ3 – Equiripple type FIR filter** - 25 taps filter with $W_p = 0.10$, $W_s = 0.20$ normalized from 0 to 1, 50 taps filter with $W_p = 0.10$, $W_s = 0.13$ normalized from 0 to 1 and 75 taps filter with $W_p = 0.10$, $W_s = 0.12$ normalized from 0 to 1 are considered for analysis.

***LS3 – Least square type FIR filter** - 25 taps filter with W_p = 0.10, W_s = 0.20 normalized from 0 to 1, 50 taps filter with W_p = 0.10, W_s = 0.13 normalized from 0 to 1 and 75 taps filter with W_p = 0.10, W_s = 0.12 normalized from 0 to 1 are considered for analysis.
* **Hamming and Bohman type FIR filter** with W_c = 0.12 for 25, 50 and 75 taps filter are considered for analysis.

Table 2: Average power saving ratio (1 – P_r) % in speech signal case.

Type	25 taps (W_p = 0.10, W_s = 0.38) Normalized (0 to 1)	50 taps (W_p = 0.10, W_s = 0.26) Normalized (0 to 1)	75 taps (W_p = 0.10, W_s = 0.20) Normalized (0 to 1)
	Power saving (1-P_r) %	Power saving (1-P_r) %	Power saving (1-P_r) %
Equiripple	21.861%	33.73%	41.31%
Least square	21.46%	33.57%	43.45%
Type	25 taps (W_p = 0.10, W_s = 0.20) Normalized (0 to 1)	50 taps (W_p = 0.10, W_s = 0.155) Normalized (0 to 1)	75 taps (W_p = 0.10, W_s = 0.135) Normalized (0 to 1)
	(1-P_r) %	(1-P_r) %	(1-P_r) %
Equiripple	9.18%	20.42%	29.92%
Least square	9.03%	25.26%	33.18%
Type	25 taps (W_p = 0.10, W_s = 0.20) Normalized (0 to 1)	50 taps (W_p = 0.10, W_s = 0.13) Normalized (0 to 1)	75 taps (W_p = 0.10, W_s = 0.12) Normalized (0 to 1)
	(1-P_r) %	(1-P_r) %	(1-P_r) %
Equiripple	16.54%	12.64%	18.02%
Least square	10.02%	16.22%	30.68%
Type	25 taps (W_c= 0.12) Normalized (0 to 1)	50 taps (W_c= 0.12) Normalized (0 to 1)	75 taps (W_c = 0.12) Normalized (0 to 1)
	(1-P_r) %	(1-P_r) %	(1-P_r) %
Hamming	26.68%	34.54%	43.60%
Bohman	26.92%	38.28%	43.64%

***W_p is the pass band frequency, W_s is the stop band frequency, W_c is the cut-off frequency normalized (0 to 1)**

From Table. 3, it is evident that the average power saving (1 - P_r) % is 43.60% for 75 taps Hamming filter. Fig.8 shows the power saving comparison between the existing technique mentioned in [34] and the proposed technique. The reason for considering only the existing technique [34] for comparison has already been discussed in section 5.4.2.2.

From the Fig.8, it is inferred that the average power saving ratio for the proposed scheme is more when compared to the existing technique for various FIR filter characteristics and the best result is obtained for the 75 taps Bohman window FIR filter characteristics. The proposed scheme average power saving ratio for Bohman filter characteristics is about 43.64%, indicates that the proposed technique provides 1.16% more power saving when compared to the other existing technique. As the taps increase, the number of filter coefficients also increases. This in turn, makes the number of multipliers turning off to gradually increase from 25 taps to 75 taps due to the linear symmetric FIR filter consideration.

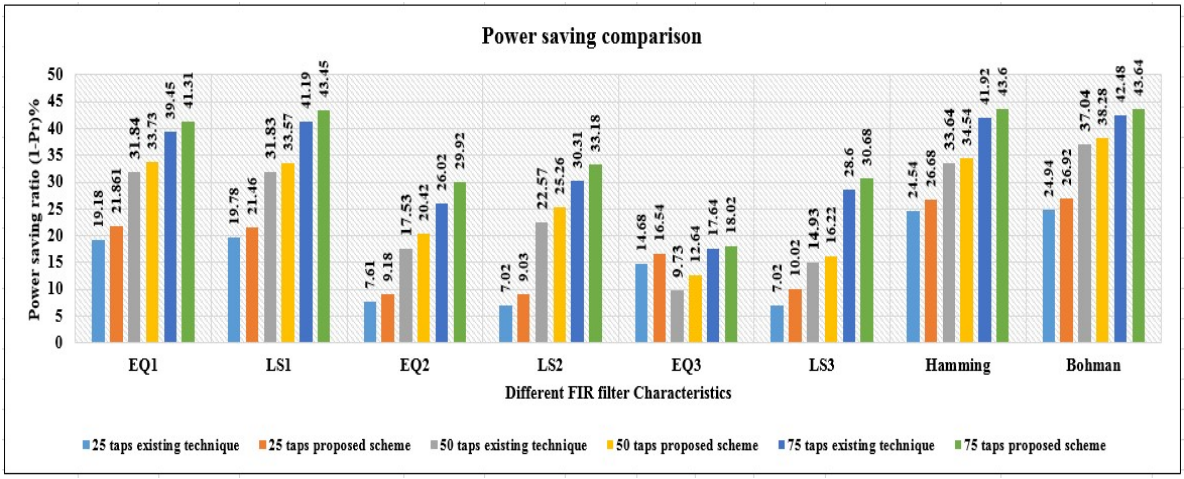


Fig. 8: Comparison of average power saving ratio between the proposed and the existing technique

Table 3: Average MSE of filter output for the implemented FIR filters.

Type	25 taps (W_p = 0.10, W_s = 0.38) Normalized (0 to 1)	50 taps (W_p = 0.10, W_s = 0.26) Normalized (0 to 1)	75 taps (W_p = 0.10, W_s = 0.20) Normalized (0 to 1)
	MSE (decibel)	MSE (decibel)	MSE (decibel)
Equiripple	-90.33	-90.57	-86.93
Least square	-91.12	-90.22	-88.55
Type	25 taps (W_p = 0.10, W_s = 0.20) Normalized (0 to 1)	50 taps (W_p = 0.10, W_s = 0.155) Normalized (0 to 1)	75 taps (W_p = 0.10, W_s = 0.135) Normalized (0 to 1)
	MSE (decibel)	MSE (decibel)	MSE (decibel)
Equiripple	-97.76	-86.47	-84.77
Least square	-96.74	-90.51	-84.78
Type	25 taps (W_p = 0.10, W_s = 0.20) Normalized (0 to 1)	50 taps (W_p = 0.10, W_s = 0.13) Normalized (0 to 1)	75 taps (W_p = 0.10, W_s = 0.12) Normalized (0 to 1)
	MSE (decibel)	MSE (decibel)	MSE (decibel)
Equiripple	-94.63	-96.42	-90.57
Least square	-95.79	-88.78	-82.43
Type	25 taps (W_c= 0.12) Normalized (0 to 1)	50 taps (W_c= 0.12) Normalized (0 to 1)	75 taps (W_c = 0.12) Normalized (0 to 1)
	MSE (decibel)	MSE (decibel)	MSE (decibel)
Hamming	-93.22	-92.53	-89.49
Bohman	-99.56	-88.77	-90.29

* W_p is the pass band frequency, W_s is the stop band frequency, W_c is the cut-off frequency normalized (0 to 1)

The Mean Square Error (MSE) represents the cumulative squared error between the proposed reconfigurable filter output and the original output. The original output is defined as the output obtained from the FIR filter without turning off the multipliers. MSE values are presented in the Table.3, which shows that there is a minor degradation in the filter performance. As the taps are increased the power saving ratio is increased because the number of multipliers turning off is increased and this leads to the slight increase in the MSE values.

Fig.9 shows the comparison of the average MSE for the proposed and the other existing technique for various FIR filter characteristics by considering 25taps, 50 taps and 75 taps FIR filter structures. In general, MSE is a measure of the differences between values predicted by a model or an estimator and the values actually observed from the thing being modeled or estimated. Since the MSE is a good measure of accuracy, it is ideal if it is small.

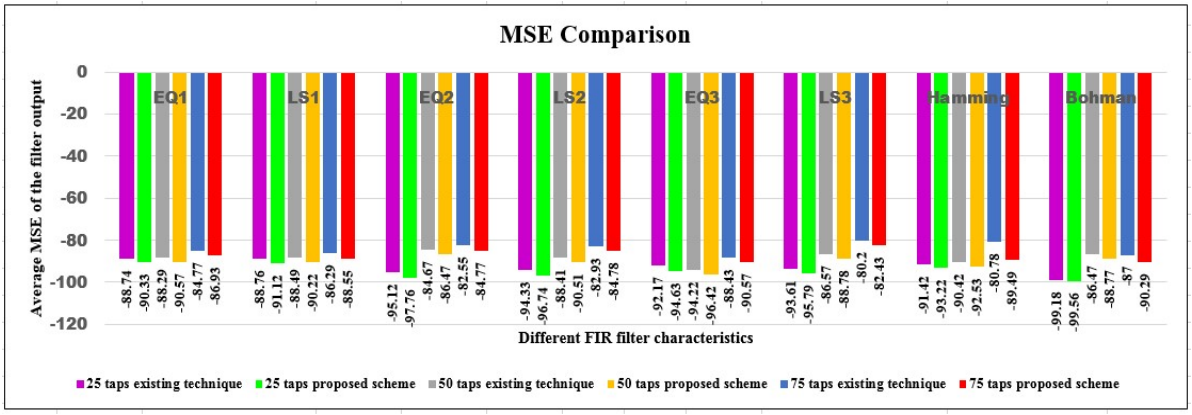


Fig. 9: Comparison of MSE between the proposed and the existing technique

From Fig.9, it is inferred that the proposed scheme MSE value is small when compared to the other existing technique. For example, in the proposed 75 taps Bohman reconfigurable FIR filter characteristics has MSE value of -90.29, which is a small when compared to the existing reconfigurable FIR filter value which is -87. As the tap increases, the MSE value slightly increases and this can be considered as a trade off in the filter performance.

Since it is an ASIC implementation, the area has been measured in mm^2 for the proposed technique as well as the existing methods namely [2], [3], [4], [5] and [34] is shown in Table.4.

Table 4: Area comparison between proposed and existing reconfiguration scheme.

Filter type	Tech [µm]	Area [mm^2]		
		25 taps	50 taps	75 taps
Proposed method [fig. 2]	0.18	0.1983	0.2329	0.3823
Ludwig et al.[2]	0.18	0.2173	0.3598	0.6016
Chen et al. [3]	0.18	0.2356	0.3525	0.6183
Yu et al. [4]	0.18	0.2571	0.3624	0.6208
Hwang et al. [5]	0.18	0.2521	0.3247	0.5542
Seok et al. [34]	0.18	0.2069	0.2629	0.5218
Chen et al.[37]	0.18	0.2023	0.2514	0.4598

In the proposed reconfigurable FIR filter, EDMB is used instead of the multiplier which makes the area utilization

by the architecture to be small when compared to the other existing techniques which uses multiplier block.

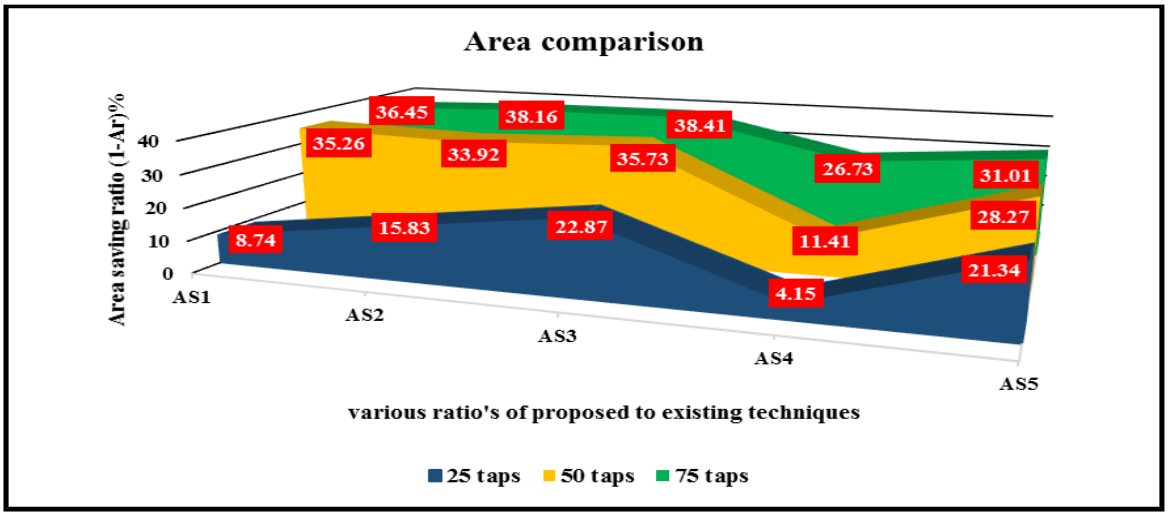


Fig. 10: Area Saving Ratio of various filter taps

Fig.10 shows the area saving ratio for various filter taps. From eqn (14), Area Saving Ratio (ASR) of various characteristics of low pass FIR filter are calculated. Ref [2],[3],[4],[5] and [34] are considered as existing techniques for finding the respective area saving ratio. The notations AS1, AS2, AS3, AS4 and AS5 used in the Fig. 10 are described as follows:

- AS1 is the area saving ratio between proposed DRS and existing technique [2]
  AS1 = 1 – (area of the proposed DRS filter / area of the existing technique [2])
- AS2 is the area saving ratio between proposed DRS and existing technique [3]
  AS2 = 1 – (area of the proposed DRS filter / area of the existing technique [3])
- AS3 is the area saving ratio between proposed DRS and existing technique [4]
  AS3 = 1 – (area of the proposed DRS filter / area of the existing technique [4])
- AS4 is the area saving ratio between proposed DRS and existing technique [34]
  AS4 = 1 – (area of the proposed DRS filter / area of the existing technique [34])
- AS5 is the area saving ratio between proposed DRS and existing technique [5]
  AS5 = 1 – (area of the proposed DRS filter / area of the existing technique [5]).

From the Fig.10, it may be seen that the ASR value of the proposed scheme is better when compared to the other existing techniques.

As the filter tap increases the area saving ratio also increases. It is clear from the Fig.10 that in the 75taps, the filter area saving is more when compared to the 25 taps and 50 taps filter. Here the filter performance increases and the clear noise free speech signal is obtained in the filter output.

In Table.5, the proposed architecture is compared with previous works [2], [3], [4], [5], [34] in terms of MSE, and Power Saving Ratio (1-Pr) %. Power Saving Ratio is normalized with the number of taps, input samples and coefficients, process technology, supply voltage and clock frequency using the eqn [22]:

$$P(Tap) = \frac{\text{Total power}}{\#taps} \times \frac{16}{\#\text{ bits coeff}} \times \frac{16}{\#\text{bits sample}} \times \left(\frac{2.5}{V_{dd}}\right)^2 \times \frac{0.25}{\text{Tech}} \times \frac{100}{\text{Clk freq}} P(Tap) = \frac{\text{Total power}}{\#taps} \times \frac{16}{\#\text{ bits coeff}} \times \frac{16}{\#\text{bits sample}} \times \left(\frac{2.5}{V_{dd}}\right)^2 \times \frac{0.25}{\text{Tech}} \times \frac{100}{\text{Clk freq}} \quad (22)$$

Table 5: Comparison of power reduction of proposed 75-tap Hamming filter with previous works.

Techniques	Filter description	Tech [µm]	Total Power	P(tap)	1-Pr	MSE (decibel)	DAT (ns)
Ludwig et al.[2]	75 taps, 16 x 16	0.18	483 mW @ 5V, 100MHz	11.64	65.15% (39.98%)	-32.91 (-39.49)	1.48
Chen et al. [3]	75 taps, 16 x 16	0.18	168 mW @ 5 V, 100 MHz	16.13	NA	NA	1.32
Yu et al. [4]	75 taps, 16 x 16	0.18	320mW @ 5 V, 100 MHz	NA	34%	NA	1.35
Hwang et al. [5]	75 taps, 16 x 16	0.18	268mW @ 5 V, 100 MHz	13.5	26%	NA	1.25
Seok et al. [34]	75 taps, 16 x 16	0.18	453mW @ 5V, 100 MHz	8.46	41.92%	-80.78	1.19
Proposed method	75 taps, 16 x 16	0.18	95.118mW @ 5 V, 100 MHz	4.403	43.60%	-89.49	1.15

DAT- Data Arrival Time; NA – Not Applicable

Table. 5 shows the comparison of power reduction in various filters with proposed filter. The reconfigurable filter in [2] consumes less power than [5]; however, MSE is even larger.

Hence finally by various analysis it may be seen that the proposed DRS fir filter gives better noise free filtered speech signal at the output and the performance analysis in terms of area saving and power saving is superior for the proposed scheme when compared to the other existing reconfiguration techniques.

6.0 CONCLUSION

In this paper, a low power and low area reconfigurable FIR filter architecture to allow efficient trade-off between the filter performance and computation energy, is discussed. In the proposed reconfigurable filter, the multipliers in the filter are turned off when the coefficients are small enough so as to mitigate the effect on the filter output. Therefore, the proposed reconfigurable filter dynamically changes the filter order to achieve significant power savings with minor degradation in the performance. Further, the efficiency of the proposed DRS which is implemented on Xilinx Virtex 7 device and is later synthesized with Cadence RTL complier using TSMC 180 nm standard cell library has been determined. The proposed scheme achieves a power saving of about 43.60% and area reduction of about 6.34% for 75 taps filter with very graceful degradation in the filter output.

Phonetic signal processing system is a good application to use the proposed reconfigurable filtering approach. The proposed work is focussed on fixed coefficients, but it can be extended to the adaptive filter cases, where both data inputs and coefficients amplitude should be monitored simultaneously. The proposed approach can be applicable to other areas of signal processing, where a proper trade-off between power savings and performance degradation

should be carefully considered. The idea presented in this paper can assist in the design of FIR filters and its implementation for low power applications.

Future work can be extended to the design of an adaptive reconfigurable FIR filter by varying the weighting strategies.

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